



NILASAIL INSTITUTE OF SCIENCE & TECHNOLOGY
SERGARH-756060, BALASORE (ODISHA)
(Approved by AICTE & affiliated to SCTE & VT, Odisha)



LESSON PLAN

SUBJECT: Th-2 (DIGITAL ELECTRONICS & MICROPROCESSOR)

CHAPTERWISE DISTRIBUTION OF PERIODS

Sl.No.	Name of the chapter as per the Syllabus	No. of Periods as per the Syllabus	No. of periods actually needed
1	Basics Of Digital Electronics	15	15
2	Combinational Logic Circuits	15	15
3	Sequential Logic Circuits	15	8
4	8085 Microprocessor	20	20
5	Interfacing And Support Chips	10	10
TOTAL		75	75

sciipline: EEE	Semester: 5 th	NameoftheTeachingFaculty:Er.RANJAN KUMAR PADHI
Week	ClassDay	Theory/PracticalTopics
1 st	1 st	1.BASICSOFDIGITALELECTRONICS 1.1 Binary, Octal,HexadecimalnumbersystemsandcomparewithDecimal system.
	2 nd	1.1Binary,Octal,Hexadecimalnumbersystemsandcomparewith Decimal system
	3 rd	1.1Binary,Octal,Hexadecimalnumbersystemsandcomparewith Decimal system
	4 th	1.2Binaryaddition,subtraction,MultiplicationandDivision.
	5 th	1.31'scomplementand2'scomplementnumbersforabinarynumber
2 nd	1 st	1.4Subtractionofbinarynumbersin2'scomplement method.
	2 nd	1.5UseofweightedandUn-weightedcodes&writeBinaryequivalent numberforanumberin8421,Excess-3andGrayCodeandvice-versa.
	3 rd	1.6ImportanceofparityBit.
	4 th	1.7LogicGates:AND,OR,NOT,NAND,NORandEX-ORgateswith truth table.
	5 th	1.7LogicGates:AND,OR,NOT,NAND,NORandEX-ORgateswith truth table.
3 rd	1 st	1.8RealizeAND,OR,NOToperationsusingNAND,NORgates.
	2 nd	1.9DifferentpostulatesandDe-Morgan'stheoremsinBooleanalgebra.
	3 rd	1.10UseOfBooleanAlgebraForSimplificationOfLogicExpression
	4 th	1.11KarnaughMapFor2,3,4Variable,SimplificationOfSOPAndPOS Logic Expression Using K-Map.
	5 th	1.11KarnaughMapFor2,3,4Variable,SimplificationOfSOPAndPOS Logic Expression Using K-Map.

4 th	1st	2. COMBINATIONAL LOGIC CIRCUITS Give the concept of combinational logic circuits.
	2nd	2.2 Half adder circuit and verify its functionality using truth table.
	3rd	2.2 Half adder circuit and verify its functionality using truth table.
	4th	2.3 Realize a Half-adder using NAND gates only and NOR gates only.
	5th	2.4 Full adder circuit and explain its operation with truth table.
5 th	1st	2.4 Full adder circuit and explain its operation with truth table.
	2 nd	2.5 Realize full-adder using two Half-adders and an OR-gate and write truth table
	3 rd	2.6 Full subtractor circuit and explain its operation with truth table.
	4 th	2.6 Full subtractor circuit and explain its operation with truth table.
	5 th	2.7 Operation of 4X1 Multiplexers and 1X4 demultiplexer
6 th	1 st	2.7 Operation of 4X1 Multiplexers and 1X4 demultiplexer
	2 nd	2.8 Working of Binary-Decimal Encoder & 3X8 Decoder.
	3 rd	2.8 Working of Binary-Decimal Encoder & 3X8 Decoder.
	4 th	2.9 Working of Two-bit magnitude comparator.
	5 th	2.9 Working of Two-bit magnitude comparator.
7 th	1 st	3. SEQUENTIAL LOGIC CIRCUITS Give the idea of Sequential logic circuits.
	2 nd	3.2 State the necessity of clock and give the concept of level clocking and edge triggering,
	3 rd	3.3 Clocked SR flip flop with preset and clear inputs.
	4th	3.5 Construct level clocked JK flip flop using S-R flip-flop and explain with truth table
	5 th	3.6 Concept of race around condition and study of master-slave JK flip flop.
8 th	1 st	3.7 Give the truth tables of edge-triggered D and T flip flops and draw their symbols.
	2 nd	3.8 Application of flip flops. 3.9 Define modulus of a counter
	3 rd	3.10 4-bit asynchronous counter and its timing diagram.
	4 th	3.10 4-bit asynchronous counter and its timing diagram.
	5 th	3.11 Asynchronous decade counter.

9 th	1 st	3.124-bitsynchronouscounter.
	2 nd	3.13Distinguishbetweensynchronousand asynchronouscounters.
	3 rd	3.14StatetheneedforaRegisterandlistthefourtypesofregisters.
	4 th	3.15WorkingofSISO,SIPO,PISO,PIPORegisterwithtruthtable using flip flop.
	5 th	3.15WorkingofSISO,SIPO,PISO,PIPORegisterwithtruthtable using flip flop.
10 th	1 st	4. 8085MICROPROCESSOR IntroductiontoMicroprocessors, Microcomputers
	2 nd	4.2ArchitectureofIntel8085AMicroprocessoranddescriptionofeach block.
	3 rd	4.2ArchitectureofIntel8085AMicroprocessoranddescriptionofeach block.
	4 th	4.2ArchitectureofIntel8085AMicroprocessoranddescriptionofeach block.
	5 th	4.3Pindiagramanddescription.
11 th	1 st	4.3Pindiagramanddescription.
	2 nd	4.3Pindiagramanddescription.
	3 rd	4.4Stack,Stackpointer&stacktop
	4 th	4.5Interrupts
	5 th	4.6Opcode&Operand,
12 th	1 st	4.7Differentiatebetweenonebyte,two byte&threebyteinstruction with example.
	2 nd	4.8Instructionsetof8085example
	3 rd	4.9Addressingmode
	4 th	4.9Addressingmode
	5 th	4.10FetchCycle,MachineCycle,InstructionCycle,T-State
	1 st	4.11TimingDiagramformemoryread,memorywrite,I/Oread,I/O write

13 th	2 nd	4.11 Timing Diagram for memory read, memory write, I/O read, I/O write
	3 rd	4.12 Timing Diagram for 8085 instruction
	4 th	4.13 Counter and time delay.
	5 th	4.14 Simple assembly language programming of 8085.
14 th	1 st	5. INTERFACING AND SUPPORT CHIPS Basic Interfacing Concepts, Memory mapping & I/O mapping
	2 nd	Basic Interfacing Concepts, Memory mapping & I/O mapping
	3 rd	Basic Interfacing Concepts, Memory mapping & I/O mapping
	4 th	5.2 Functional block diagram and description of each block of Programmable peripheral interface Intel 8255
	5 th	5.2 Functional block diagram and description of each block of Programmable peripheral interface Intel 8255
15 th	1 st	5.2 Functional block diagram and description of each block of Programmable peripheral interface Intel 8255
	2 nd	5.2 Functional block diagram and description of each block of Programmable peripheral interface Intel 8255
	3 rd	5.3 Application using 8255: Seven segment LED display, Square wave generator, Traffic light Controller
	4 th	5.3 Application using 8255: Seven segment LED display, Square wave generator, Traffic light Controller
	5 th	5.3 Application using 8255: Seven segment LED display, Square wave generator, Traffic light Controller