NILASAILA INSTITUTE OF SCIENCE & TECHNOLOGY
SERGARH-756060, BALASORE (ODISHA)
(Approved by AICTE& affiliated to SCTE&VT, Odisha)

NIST POLYTECHNIC

LESSON PLAN

SUBJECT: DIGITAL ELECTRONICS & MICROPROCESSOR(Th-3)

Name Of The Faculty :- Er.Prakash kumar Mohanty
Branch :- Electrical & Electronics Engg. **Semester :-** 5th
Session :- 2024-25 **Examination :-** 2024 (W)

CHAPTER WISE DISTRIBUTION OF PERIODS

Sl.No.	Name of the chapter as per the Syllabus	No. of Periods as per the Syllabus	No. of periods actually needed
1	Basics Of Digital Electronics	15	16
2	Combinational Logic Circuits	15	16
3	Sequential Logic Circuits	15	16
4	8085 Microprocessor	20	20
5	Interfacing And Support Chips	10	11
Total periods		75	79

Sign of Faculty

Sign of H.O.D.

Discipline: EEE	Semester: 5th	Name of the Teaching Faculty: Er.Biswajit Parida
		SESSION : 2024-25 EXAMINATION : 2024 (S)
Week	**Class Day**	**Theory / Practical Topics**
1st	1st	1. BASICS OF DIGITAL ELECTRONICS 1.1 Binary, Octal, Hexadecimal number systems and compare with Decimal system.
	2nd	1.2 Binary addition, subtraction, Multiplication and Division.
	3rd	1.2 Binary addition, subtraction, Multiplication and Division.
	4th	1.3 1's complement and 2's complement numbers for a binary number
	5th	1.4 Subtraction of binary numbers in 2's complement method.
2nd	1st	1.5 Use of weighted and Un-weighted codes & write Binary equivalent number for a number in 8421, Excess-3 and Gray Code and vice-versa.
	2nd	1.6 Importance of parity Bit.
	3rd	1.7 Logic Gates: AND, OR, NOT, NAND, NOR and EX-OR gates with truth table.
	4th	1.7 Logic Gates: AND, OR, NOT, NAND, NOR and EX-OR gates with truth table.
	5th	1.8 Realize AND, OR, NOT operations using NAND, NOR gates.
3rd	1st	1.8 Realize AND, OR, NOT operations using NAND, NOR gates.
	2nd	1.9 Different postulates and De-Morgan's theorems in Boolean algebra.
	3rd	1.9 Different postulates and De-Morgan's theorems in Boolean algebra.
	4th	1.10 Use Of Boolean Algebra For Simplification Of Logic Expression
	5th	1.11 Karnaugh Map For 2,3,4 Variable, Simplification Of SOP And POS Logic Expression Using K-Map.
4th	1st	1.11 Karnaugh Map For 2,3,4 Variable, Simplification Of SOP And POS Logic Expression Using K-Map.
	2nd	2. COMBINATIONAL LOGIC CIRCUITS 2.1 Give the concept of combinational logic circuits.
	3rd	2.2 Half adder circuit and verify its functionality using truth table.
	4th	2.2 Half adder circuit and verify its functionality using truth table.
	5th	2.3 Realize a Half-adder using NAND gates only and NOR gates only.

Week	Class Day	Theory / Practical Topics
5th	1st	2.3 Realize a Half-adder using NAND gates only and NOR gates only.
	2nd	2.4 Full adder circuit and explain its operation with truth table
	3rd	2.4 Full adder circuit and explain its operation with truth table
	4th	2.5 Realize full-adder using two Half-adders and an OR – gate and write truth table
	5th	2.5 Realize full-adder using two Half-adders and an OR – gate and write truth table
6th	1st	2.6 Full subtractor circuit and explain its operation with truth table.
	2nd	2.7 Operation of 4 X 1 Multiplexers and 1 X 4 demultiplexer
	3rd	2.7 Operation of 4 X 1 Multiplexers and 1 X 4 demultiplexer
	4th	2.8 Working of Binary-Decimal Encoder & 3 X 8 Decoder
	5th	2.8 Working of Binary-Decimal Encoder & 3 X 8 Decoder
7th	1st	2.9 Working of Two bit magnitude comparator.
	2nd	2.9 Working of Two bit magnitude comparator.
	3rd	3. SEQUENTIAL LOGIC CIRCUITS 3.1 Give the idea of Sequential logic circuits.
	4th	3.2 State the necessity of clock and give the concept of level clocking and edge triggering,
	5th	3.3 Clocked SR flip flop with preset and clear inputs.
8th	1st	3.5 Construct level clocked JK flip flop using S-R flip-flop and explain with truth table
	2nd	3.6 Concept of race around condition and study of master slave JK flip flop.
	3rd	3.6 Concept of race around condition and study of master slave JK flip flop.
	4th	3.7 Give the truth tables of edge triggered D and T flip flops and draw their symbols.
	5th	3.8 Applications of flip flops.

Week	Class Day	Theory / Practical Topics
9th	1st	3.9 Define modulus of a counter
	2nd	3.10 4-bit asynchronous counter and its timing diagram.
	3rd	3.11 Asynchronous decade counter
	4th	3.12 4-bit synchronous counter.
	5th	3.13 Distinguish between synchronous and asynchronous counters.
10th	1st	3.14 State the need for a Register and list the four types of registers
	2nd	3.15 Working of SISO, SIPO, PISO, PIPO Register with truth table using flip flop.
	3rd	3.15 Working of SISO, SIPO, PISO, PIPO Register with truth table using flip flop.
	4th	4. 8085 MICROPROCESSOR 4.1 Introduction to Microprocessors, Microcomputers
	5th	4.2 Architecture of Intel 8085A Microprocessor and description of each block.
11th	1st	4.2 Architecture of Intel 8085A Microprocessor and description of each block.
	2nd	4.3 Pin diagram and description.
	3rd	4.3 Pin diagram and description.
	4th	4.4 Stack, Stack pointer & stack top
	5th	4.5 Interrupts
12th	1st	4.6 Opcode & Operand,
	2nd	4.7 Differentiate between one byte, two byte & three byte instruction with example.
	3rd	4.8 Instruction set of 8085 example
	4th	4.8 Instruction set of 8085 example
	5th	4.9 Addressing mode
13th	1st	4.9 Addressing mode
	2nd	4 .10 Fetch Cycle, Machine Cycle, Instruction Cycle, T-State
	3rd	4.11 Timing Diagram for memory read, memory write, I/O read, I/O write
	4th	4.11 Timing Diagram for memory read, memory write, I/O read, I/O write
	5th	4.12 Timing Diagram for 8085 instruction

Week	Class Day	Theory / Practical Topics
14th	1st	4.13 Counter and time delay.
	2nd	4. 14 Simple assembly language programming of 8085.
	3rd	4. 14 Simple assembly language programming of 8085.
	4th	5. INTERFACING AND SUPPORT CHIPS 5.1 Basic Interfacing Concepts, Memory mapping & I/O mapping
	5th	5.1 Basic Interfacing Concepts, Memory mapping & I/O mapping
15th	1st	5.2 Functional block diagram and description of each block of Programmable peripheral interface Intel 8255
	2nd	5.2 Functional block diagram and description of each block of Programmable peripheral interface Intel 8255
	3rd	5.2 Functional block diagram and description of each block of Programmable peripheral interface Intel 8255
	4th	5.2 Functional block diagram and description of each block of Programmable peripheral interface Intel 8255
	5th	5.3 Application using 8255: Seven segment LED display, Square wave generator, Traffic light Controller
16	1st	5.3 Application using 8255: Seven segment LED display, Square wave generator, Traffic light Controller
	2nd	5.3 Application using 8255: Seven segment LED display, Square wave generator, Traffic light Controller
	3rd	5.3 Application using 8255: Seven segment LED display, Square wave generator, Traffic light Controller
	4th	5.3 Application using 8255: Seven segment LED display, Square wave generator, Traffic light Controller

SIGN. OF HOD

SIGN. OF FACULTY