NILASAILA INSTITUTE OF SCIENCE & TECHNOLOGY
SERGARH-756060, BALASORE (ODISHA)
(Approved by AICTE& affiliated to SCTE&VT, Odisha)

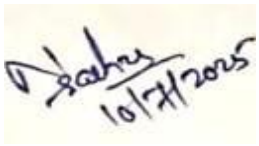
LESSON PLAN

SUBJECT: EEEPC-205(DIGITAL ELECTRONICS)

Name Of The Faculty :- Er.Niranjan Sahu
Branch :- Electrical & Electronics Engg. **Semester :-** 3rd
Academic Year : 2025-26 **Examination :-** 2025 (w)

CHAPTER WISE DISTRIBUTION OF PERIODS

Sl.No.	Name of the chapter as per the Syllabus	No. of Periods as per the Syllabus	No. of periods actually needed
1	Logic Gates	4	6
2	Boolean Algebra	5	7
3	Combinational Logic Circuits	6	8
4	Latches & Flip-Flops	6	8
5	Counters	7	9
6	Shift Registers	5	7
7	Semiconductor Memories	7	9
8	Sequential Circuit Design	5	6
	Total Period:	45	60



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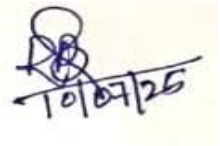

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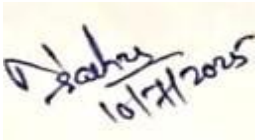
Name of the programme: Diploma in Electrical & Electronics Engg.	Semester: 3rd	**Name of the Teaching Faculty:** Er.Niranjan Sahu	
		Academic Year : 2025-26 **Examination :** 2025 (W)	
Course Code: EEEPC-205(TH-3)	**Course Year:** Second Year	**No. of Classes Alloted Per Week :**	4
		Planned Classes Required to Complete the Course	60

Week	Class Day	Topics to be Covered
1st	1st	**Logic Gates** 1.1 Basic logic gates: OR, AND, and NOT 1.1.1 Truth tables 1.1.2 Logic symbols
	2nd	1.1.3 Logic voltage levels 1.1.4 Logic circuit design examples
	3rd	1.2 Integrated Circuits 1.3 NOR, NAND, Exclusive OR, and Exclusive NOR gates.
	4th	1.4 NOR and NAND gates used as inverters.
2nd	1st	1.5 Fan-in and fan-out
	2nd	1.6 Termination of unused inputs 1.7 AND and OR gates constructed from NAND and NOR gates
	3rd	**Boolean Algebra** 2.1 Boolean operations (OR, AND, NOT) 2.2 Representation of logic circuits by Boolean expressions.
	4th	2.3 Laws of Boolean algebra: 2.3.1 Double inversion: A"=A 2.3.2 OR identities: A+0 = A, A+1=1, A+A=A, A+A'=1
3rd	1st	2.3.3 AND identities: A.0=0, A.1=A, A.A=A, A.A'=0 2.3.4 Cumulative laws: A+B=B+A, A.B=B.A 2.3.5 Associative laws:(A+B)+C=A+(B+C), (A.B).C=A.(B.C)
	2nd	2.3.6 Distributive laws: A+(B.C)=(A+B).(A+C), A.(B+C)=A.B+A.C 2.3.7 DeMorgan's theorems :(A+B+C+...)'=A'.B'.C'...,(A.B.C...)'=A'+B'+C'...
	3rd	2.3.8 Applications to logic circuit simplifications and design 2.4 Equivalent logic gates 2.5 NAND and NOR implementations of logic circuits.
	4th	2.6 Standard forms of Boolean expressions 2.6.1 Sum-of-products (SOP) 2.6.2 Product-of-sums (POS)

Week	Class Day	Topics to be Covered
4th	1st	2.7 Karnaugh mapping
	2nd	**Combinational Logic Circuits** 3.1 Half adder 3.2 Full adder
	3rd	3.3 Half Subtractor 3.4 Full Subtractor
	4th	3.5 4 bit adder. 3.6 Multiplexer (4:1)
5th	1st	3.7 De- multiplexer (1:4)
	2nd	3.8 Decoder 3.9 Encoder
	3rd	3.10 Digital comparator (3 Bit)
	4th	3.11 Seven segment Decoder
6th	1st	Revision on Full Subtractor
	2nd	**Latches & Flip-Flops** 4.1. Basic latches 4.1.1 NOR latch
	3rd	4.1.2 NAND latch 4.1.3 Example uses of latches
	4th	Latches & Flip-Flops 4.1. Basic latches
7th	1st	4.1.2 NAND latch 4.1.3 Example uses of latches
	2nd	4.2. Gated latches 4.2.1 Gated S-R latch 4.2.2 Gated D-latch
	3rd	4.3. Flip-flops: 4.3.1 Master-slave and edge-triggered principles
	4th	4.3.2 S-R flip-flop 4.3.3 D-type flip-flop 4.3.4 J-K flip-flop
8th	1st	4.3.5 T-type flip-flop 4.3.6 Flip-flop timing diagrams
	2nd	**Counters** 5.1 Circuit diagram and working principle of Binary counters
	3rd	5.2 up-down counter (circuits, truth tables, and timing diagrams)
	4th	5.3 Asynchronous counters and ripple counter
9th	1st	5.4 Synchronous counters
	2nd	5.5 Decade counter
	3rd	5.6 Module–n counter and its combinations
	4th	5.7. Divide-by-n counters obtained from truncated binary sequences 5.8. Synchronous counter design using D-type flip-flops

Week	Class Day	Topics to be Covered
10th	1st	5.9 Synchronous counter design using J-K flip-flops
	2nd	Revision on Synchronous counters
	3rd	**Shift Registers** 6.1 Circuit diagram, truth tables, and timing diagrams of Shift Registers
	4th	6.2 Serial input shift register
11th	1st	6.3 Serial/parallel load shift register
	2nd	6.4 Shift register counters 6.4.1. Ring counter
	3rd	6.4.2. Self-starting ring counter
	4th	6.4.2. Self-starting ring counter
12th	1st	6.4.3. Johnson counter
	2nd	**Semiconductor Memories** 7.1 Define the terms ROM, RAM, PROM, EPROM.
	3rd	7.2 Draw a typical memory cell
	4th	7.3 Design a small diode matrix ROM to serve as a code converter.
13th	1st	7.4 Design and draw the logic diagram of a specified size memory system
	2nd	7.4 Design and draw the logic diagram of a specified size memory system
	3rd	7.5 Operating principle of dynamic memory
	4th	7.6 Advantages and disadvantages of dynamic memory vs. static memory
14th	1st	7.7 Difference between dynamic memory vs. static memory
	2nd	Revision on Operating principle of dynamic memory
	3rd	**Sequential Circuit Design** 8.1 Combinational vs. Sequential circuits
	4th	8.1 Combinational vs. Sequential circuits
15th	1st	8.2 Adder, Subtractor, decoder, multiplexer, de-multiplexer, and comparator
	2nd	8.2 Adder, Subtractor, decoder, multiplexer, de-multiplexer, and comparator
	3rd	8.3. Finite state machines- Concept only
	4th	Revision on Finite state machines



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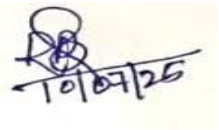

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